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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/886,823 | 06/21/2001 | Andres Bryant | BUR920000059US1 | 6851 |
| 23123 | 7590 | 07/23/2004 | EXAMINER | |
| SCHMEISER OLSEN & WATTS 18 E UNIVERSITY DRIVE SUITE # 101 MESA, AZ 85201 | | | ABRAHAM, FETSUM | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2826 | |

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/886,823

Applicant(s)

BRYANT ET AL.

Examiner

Fetsum Abraham

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-30,32 and 34-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 36-40 is/are allowed.
- 6) ☒ Claim(s) the rest is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Art Unit: 2826

Claims rejection

As a preliminary matter, the IDS documents submitted by applicant have been considered and applicant must attach the associated PTO-FORM 1449 in the next response for official acknowledgement.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 25-30,32,34,35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt (6,586,296) in view of Melen (4,041,519).

As for claims 25,26, the primary reference discloses an N-type and a P-type transistors on a substrate having gates of different firmi levels by virtue of the difference in material used to make the gates (see column 1, 50-60).

Although it is notoriously known by the art to make transistors with vertical edges and that particular structure missing in the prior art, the secondary reference, however, clearly shows the structure as discussed in the first action. Therefore, it would have been obvious to one skilled in the art to terminate transistors with vertical edges, since straight-line cutting is the simplest method of individuating multiple transistors made on a single wafer.

As for claim 27, the claimed conductivity types of the gates are duplicates of the prior art as taught in column 1, lines 50-60.

Art Unit: 2826

As for claim 28, SOI based transistors are commercially available and preferred products compared to regular transistors specifically for their superiority in noise and leakage issues. Therefore, it would have been obvious to one skilled in the art to form transistors on insulating substrates for these advantages.

As for claim 29, the gates of the prior art are made from polysilicon materials.

As for claim 30, there is no field effect transistor without gate insulation layer between the specified layers and the transistors of the prior arts are provided with gate insulation layers at the exact claimed positions.

As for claim 32, the primary prior art has a unformed impurity body density.

As for claim 34, the formula is generic to MOSFETs and the net result of the doping density is expected to conform to the commonly accepted density in the art unless proven to be different and the criticality of the formula in producing a doping level outside the commonly accepted range of densities. Please note that substrate doping density is variable in nature that differs from a design to another based on desired conductance, resistance and other issues such as leakage characteristics and etc.

As for claim 35, transistor edges are commonly known to be formed on opposing sides and perpendicular to the bottom and top surfaces of substrates. The structure in the secondary reference also confirms to the claimed specifics.

Claims 36-40 have been allowed.

The n-type and p-type polysilicon gates of the claimed dual gated vertical transistor is neither taught nor rendered obvious by the prior art. Although PN:

Art Unit: 2826

5,032,529 may have polysilicon gates in a single dual gated vertical transistor, it, however, omits the conductivity types of the poly-gates.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Refer to PN: 5,032,529.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham

7/16/04